EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"20040015540"	US-PGPUB; USPAT	OR	OFF	2006/05/24 09:54
L2	1	"20030149795"	US-PGPUB; USPAT	OR	OFF	2006/05/24 09:54
L3	14	(san or (storage adj2 network)) and (lun with mask$3) and port and class and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/24 09:54
L4	8	storage with (port and class) near driver and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/24 09:54
L5	7	("5,790,795" "5,802,327" "5,809,224" "5,954,796" "5,960,451" "6,058,489" "6,154,854").pn.	USPAT	OR	OFF	2006/05/24 09:54
L6	40	(san or (storage adj2 network)) and (lun or (logical adj2 number)) and (host adj2 adapter) with driver and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/24 09:54
L7	43	(san or (storage adj2 network)) and (lun with (mask$3 or filter$3)) and access and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/24 09:54
L8	27	(san or (storage adj2 network)) and (lun with (mask$3 or filter$3)) and driver and access and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/24 09:54
L9	1	"6035023".pn.	USPAT	OR	OFF	2006/05/24 09:54
L10	3	(storage adj system adj coupled).ti.	USPAT	OR	OFF	2006/05/24 09:54
L11	27	(san or (storage adj2 network)) and (lun with (mask$3 or filter$3)) and driver and access and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/24 09:54

L12	7	("5,790,795" "5,802,327" "5,809, 224" "5,954,796" "5,960,451" "6, 058,489" "6,154,854").pn.	USPAT	OR	OFF	2006/05/24 09:54
L13	2	L12 and mask$3	USPAT	OR	OFF	2006/05/24 09:54
L14	33	(san or (storage adj2 network)) and ((lun or (logical adj2 number)) with (mask$3 or filter$3)) and driver and access$3 and (((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/24 09:54
L15	6	L14 not L11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/24 09:54
L16	2	"6671820".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/24 09:54
L17	4	(719/321,325-326.ccls. or 711/163.ccls.) and ((lun or (logical adj2 number)) with (mask$3 or filter$3)) and driver and access$3 and (((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/24 10:01
L20	4	(719/321,325-326.ccls. or 711/100,163.ccls. or 718/104) and ((lun or (logical adj2 number)) with (mask$3 or filter$3)) and driver and access$3 and (((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/24 10:06

Web   Images   Groups   News   Froogle   Maps   **more »**

Google | lun masking | Search | Advanced Search
Preferences

Web

Results **1 - 10** of about **418,000** for **lun** masking. (0.19 seconds)

What is **LUN masking**?
LUN Masking is implemented primarily at the HBA (Host Bus Adapater) level. **LUN Masking** implemented at this level is vulnerable to any attack that ...
www.sansecurity.com/faq/**lun-masking**.shtml - 9k - Cached - Similar pages

[PDF] **LUN Masking** in a SAN
File Format: PDF/Adobe Acrobat - View as HTML
LUN Masking is used to assign appropriately sized pieces of storage ... **LUN Masking** is the capability that allows a specific **LUN** to be exclu- ...
www.qlogic.com/documents/datasheets/
knowledge_data/whitepapers/whitepaper.**lunmasking**.pdf - Similar pages

[PDF] **LUN Masking**: The First Line of Defense
File Format: PDF/Adobe Acrobat - View as HTML
Technically speaking **LUN Masking** is a type of Authorization. – Without anything else right now ... On initial config of **LUN Masking** turn off ALL access. ...
www.snia.org/ssif/about/documents/SS_Ramos_LunMask.pdf - Similar pages

[PDF] **LUN Masking** and **LUN** Re-Mapping
File Format: PDF/Adobe Acrobat
The benefit of implementing **LUN Masking** and Re-Mapping in ... (TCO) by providing a single point where all **LUN Masking** is. implemented. ...
www.maxxan.com/product/docs/**lun_masking**.pdf - Similar pages

LUN Masking at Real-Storage
Real-Storage is a provider of intelligent Networking Data Storage Solutions.
www.real-storage.com/**lun-masking**.html - 13k - Cached - Similar pages

What is **LUN masking**?
Was our answer to What is **LUN masking**? helpful to you? Join the Tech FAQ Forum to discuss What is **LUN masking**? Bookmark What is **LUN masking**? ...
www.tech-faq.com/**lun-masking**.shtml - 21k - Cached - Similar pages

LUN masking makes for fast data recovery
Using the Volume Shadow Copy Service and Virtual Disk Service built into Windows Server 2003, you can set system restore points by creating snapshots of ...
searchwinsystems.techtarget.com/ tip/1,289483,sid68_gci1115888,00.html - 50k - Cached - Similar pages

Storage Mountain: Backup software vendors
DISC, MON & REP, **LUN MASK**, ZONE, MULT PATH, VOL MAN & VIRT, FILE SYS ...
LUN MASK: The settings of **LUN masking** configurations from a central point. ...
www.backupcentral.com/software-SAN.html - 41k - Cached - Similar pages

LUN Masking vs. Zoning
LUN masking, performed at the storage controller level, allows you to define ... **LUN masking** provides more detailed security than zoning, because LUNs ...
technet2.microsoft.com/WindowsServer/ en/Library/84c2fa21-86ac-49b0-be10-
3737af2abd6a1033.mspx - 16k - Cached - Similar pages

Build Your Own SAN
With **LUN Masking** you can use a single Fibre Channel link to split up a RAID ... **LUN Masking**, which is usually carried out by intelligent Fibre Channel RAID ...
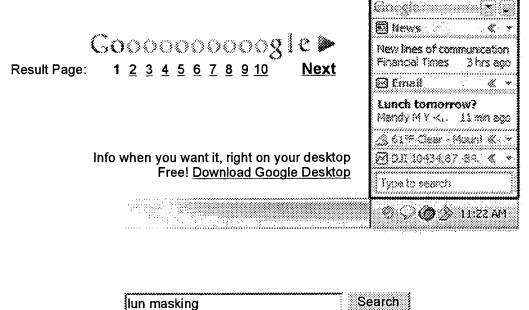
www.extremetech.com/article2/0,1697,1160867,00.asp - 88k - <u>Cached</u> - <u>Similar pages</u>

Try your search again on <u>Google Book Search</u>

Goooooooooogle ▶

Result Page: **1** <u>2</u> <u>3</u> <u>4</u> <u>5</u> <u>6</u> <u>7</u> <u>8</u> <u>9</u> <u>10</u>   **Next**

Info when you want it, right on your desktop
Free! <u>Download Google Desktop</u>

| lun masking | Search |

<u>Search within results</u> | <u>Language Tools</u> | <u>Search Tips</u> | <u>Dissatisfied? Help us improve</u>

<u>Google Home</u> - <u>Advertising Programs</u> - <u>Business Solutions</u> - <u>About Google</u>

©2006 Google

The recent database difficulties have been resolved. Please let us know if you encounter any data corruptions.

CiteSeer Find: lun masking   Documents   Citations

Searching for **PHRASE lun masking**.
Restrict to: <u>Header</u> <u>Title</u> Order by: <u>Expected citations</u> <u>Hubs</u> <u>Usage</u> <u>Date</u> Try: <u>Google (CiteSeer)</u> <u>Google (Web)</u> <u>Yahoo!</u> <u>MSN</u> <u>CSB</u> <u>DBLP</u>
Order: number of citations.

<u>Introducing A Flexible Data Transport Protocol - For Network Storage (2002)</u>   <u>(Correct)</u>
security for data transport. FC does have **LUN Masking**, but this is mostly a function of the FC
that Fibre Channel's main security mechanism is **LUN masking** which is implemented mostly on the switch.
romulus.gsfc.nasa.gov/msst/conf2002/papers/d04cp-pkh.pdf

Try your query at: <u>Google (CiteSeer)</u>   <u>Google (Web)</u>   <u>Yahoo!</u>   <u>MSN</u>   <u>CSB</u>   <u>DBLP</u>

CiteSeer.IST - Copyright <u>Penn State</u> and <u>NEC</u>

Welcom   United States Patent and Trademark Office

BROWSE   SEARCH   IEEE XPLORE GUIDE   SUPPORT

Search Results

Results for "(l gical unit number masking<in>metadata)"
Your search matched **0** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

(logical unit number masking<in>metadata)   Search >

☐ Check to search only within this results set

Display Format: ◉ Citation   ○ Citation & Abstract

No results were found.

Please edit your search criteria and try again. Refer to the Help pages if you need assistance revising your search.

PORTAL

USPTO

Search: ⦿ The ACM Digital Library   ○ The Guide

logical unit number masking

THE ACM DIGITAL LIBRARY

Feedback Report a problem Satisfaction survey

Terms used **logical** **unit** **number** **masking**

Found **101,049** of **176,279**

Sort results by   relevance ▾

Display results   expanded form ▾

⬧ Save results to a Binder

▣ Search Tips

☐ Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 1 - 20 of 200   Result page: **1** 2 3 4 5 6 7 8 9 10   next
Best 200 shown   Relevance scale ☐ ▭ ▨ ▩ ▦

1 Associative and Parallel Processors   ▦
Kenneth J. Thurber, Leon D. Wald
December 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 4
Publisher: ACM Press
Full text available: 📄 pdf(2.62 MB)   Additional Information: full citation, references, citings, index terms

2 A Systematic Methodology to Compute the Architectural Vulnerability Factors for a   ▦
High-Performance Microprocessor
Shubhendu S. Mukherjee, Christopher Weaver, Joel Emer, Steven K. Reinhardt, Todd Austin
December 2003 **Proceedings of the 36th annual IEEE/ACM International Symposium
          on Microarchitecture**
Publisher: IEEE Computer Society
Full text available: 📄 pdf(248.01 KB)   Additional Information: full citation, abstract, citings, index terms

> Single-event upsets from particle strikes have become akey challenge in microprocessor
> design. Techniques todeal with these transient faults exist, but come at a cost.Designers
> clearly require accurate estimates of processorerror rates to make appropriate
> cost/reliability trade-offs.This paper describes a method for generating theseestimates.A
> key aspect of this analysis is that some single-bit faults(such as those occurring in the
> branch predictor) will notproduce an error in a program's output ...

3 An asynchronous matrix-vector multiplier for discrete cosine transform   ▦
Kyeounsoo Kim, Peter A. Beerel, Youpyo Hong
August 2000 **Proceedings of the 2000 international symposium on Low power
          electronics and design**
Publisher: ACM Press
Full text available: 📄 pdf(400.48 KB)   Additional Information: full citation, abstract, references, index terms

> This paper proposes an efficient asynchronous hardwired matrix-vector multiplier for the
> rwo-dimensional discrete cosine transform and inverse discrete cosine transform
> (DCT/IDCT). The design achieves low power and high performance by taking advantage of
> the typically large fraction of zero and small-valued data in DCT and IDCT applications. In
> particular, it skips multiplication by zero and dynamically activates/deactivates required
> bit-slices of fine-grain bit-partitioned adders using sim ...
>
> **Keyw rds:** asynchronous matrix-vector multiplier, discrete cosine transform

4 Parallel-and-vector implementation of the event-driven logic simulation algorithm on   ▦
the Cray Y-MP supercomputer

A. Bataineh, F. Özgüner
December 1992 **Pr ceedings f the 1992 ACM/IEEE c nference n Supercomputing**
Publisher: IEEE Computer Society Press
Full text available: pdf(926.62 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>index terms</u>

---

5 <u>On Application of Output Masking to Undetectable Faults in Synchronous Sequential</u>
<u>Circuits with Design-for-Testability Logic</u>
Irith Pomeranz, Sudhakar M. Reddy
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on**
          Computer-aided design
Publisher: IEEE Computer Society
Full text available: pdf(118.58 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>index terms</u>

> Design-for-testability (DFT) for synchronous sequentialcircuits causes redundant faults in
> the original circuit to bedetectable in the circuit with DFT logic. It has beenargued that
> such faults should not be detected in order toavoid reducing the yield unnecessarily. One
> way to dealwith such faults is to mask (or ignore) their fault effectswhen they appear on
> the circuit outputs, without maskingthe detection of faults that need to be detected. To
> investigatethe extent to which this can be accom ...

---

6 <u>WISQ: a restartable architecture using queues</u>
A. R. Pleszkun, J. R. Goodman, W. C. Hsu, R. T. Joersz, G. Bier, P. Woest, P. B. Schechter
June 1987 **Proceedings of the 14th annual international symposium on Computer**
          architecture
Publisher: ACM Press
Full text available: pdf(1.14 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index</u>
                                    <u>terms</u>

> In this paper, the WISQ architecture is described. This architecture is designed to achieve
> high performance by exploiting new compiler technology and using a highly segmented
> pipeline. By having a highly segmented pipeline, a very-high-speed clock can be used.
> Since a highly segmented pipeline will require relatively long pipelines, a way must be
> provided to minimize the effects of pipeline bubbles that are formed due to data and
> control dependencies. It is also important to provide a way ...

---

7 <u>VLSI design: A novel architecture for power maskable arithmetic units</u>
L. Benini, A. Macii, E. Macii, E. Omerbegovic, M. Poncino, F. Pro
April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI**
Publisher: ACM Press
Full text available: pdf(166.52 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

> Power maskable units have been proposed as a viable solution for preventing side-
> channel attacks to cryptoprocessors. This paper presents a novel architecture for the
> implementation of a class of such kinds of units, namely arithmetic components, which
> find wide usage in cryptographic applications and which are not suitable to traditional
> masking techniques. Results of extensive exploration and architectural trade-off analysis
> show the viability of the proposed solution.
>
> **Keywords**: cryptography, low-power design, security

---

8 <u>Poster session 2: The design of the fixed point unit for the z990 microprocessor</u>
Fadi Busaba, Timothy Slegel, Steven Carlough, Christopher Krygowski, John G. Rell
April 2004 **Pr ceedings f the 14th ACM Great Lakes symposium on VLSI**
Publisher: ACM Press
Full text available: pdf(171.37 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

> The paper presents the design of the Fixed Point Unit (FXU) for the IBM eServer z990
> microprocessor (announced in 2Q '03) that runs at 1.2 GHz [2]. The FXU is capable of

executing two Register-Memory instructions including arithmetic instructions and a branch instruction in a single cycle. The FXU executes a total of 369 instructions that operate on variable size operands (1 to 256 bytes). The instruction set include decimal arithmetic with multiplies and divides, binary arithmetic, shifts and r ...

Keyw rds: microprocessor, superscalar FXU

9 General storage protection techniques: Securing distributed storage: challenges, techniques, and systems
Vishal Kher, Yongdae Kim
November 2005 **Proceedings of the 2005 ACM workshop on Storage security and survivability StorageSS '05**
Publisher: ACM Press
Full text available: pdf(294.61 KB)   Additional Information: full citation, abstract, references, index terms

The rapid increase of sensitive data and the growing number of government regulations that require longterm data retention and protection have forced enterprises to pay serious attention to storage security. In this paper, we discuss important security issues related to storage and present a comprehensive survey of the security services provided by the existing storage systems. We cover a broad range of the storage security literature, present a critical review of the existing solutions, compare ...

Keywords: authorization, confidentiality, integrity, intrusion detection, privacy

10 Adding a vector unit to a superscalar processor
Francisca Quintana, Jesus Corbal, Roger Espasa, Mateo Valero
May 1999 **Proceedings of the 13th international conference on Supercomputing**
Publisher: ACM Press
Full text available: pdf(1.75 MB)   Additional Information: full citation, references, citings, index terms

11 Toward a unified framework for version modeling in engineering databases
Randy H. Katz
December 1990 **ACM Computing Surveys (CSUR)**, Volume 22 Issue 4
Publisher: ACM Press
Full text available: pdf(3.14 MB)   Additional Information: full citation, abstract, references, citings, index terms, review

Support for unusual applications such as computer-aided design data has been of increasing interest to database system architects. In this survey, we concentrate on one aspect of such support, namely, version modeling. By this, we mean the concepts suitable for structuring a database of complex engineering artifacts that evolve across multiple representations and over time and the operations through which such artifact descriptions are created and modified. There have been ...

12 Multiscalar processors
Gurindar S. Sohi, Scott E. Breach, T. N. Vijaykumar
May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture ISCA '95**, Volume 23 Issue 2
Publisher: ACM Press
Full text available: pdf(1.44 MB)   Additional Information: full citation, abstract, references, citings, index terms

Multiscalar processors use a new, aggressive implementation paradigm for extracting large quantities of instruction level parallelism from ordinary high level language programs. A single program is divided into a collection of tasks by a combination of software and hardware. The tasks are distributed to a number of parallel processing units

which reside within a processor complex. Each of these units fetches and executes instructions belonging to its assigned task. The appearance of a single log ...

13 Multiscalar processors

Gurindar S. Sohi, Scott E. Breach, T. N. Vijaykumar

August 1998 **25 years f the internati nal symp sia n Computer architecture (selected papers)**

Publisher: ACM Press

Full text available: pdf(1.57 MB)   Additional Information: full citation, references, citings, index terms

14 Single-pass full-screen hardware accelerated antialiasing

Jin-Aeon Lee, Lee-Sup Kim

August 2000 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Publisher: ACM Press

Full text available: pdf(8.82 MB)   Additional Information: full citation, references, citings, index terms

Keywords: antialiasing, graphics hardware, parallel computing, rendering hardware

15 Regular circuit fabrics: act two-the industrial perspectives (invited): Design methodology and tools for NEC electronics' structured ASIC ISSP

Takumi Okamoto, Tsutomu Kimoto, Naotaka Maeda

April 2004 **Proceedings of the 2004 international symposium on Physical design**

Publisher: ACM Press

Full text available: pdf(324.94 KB)   Additional Information: full citation, abstract, references, index terms

In this paper, we describe a design methodology and tools for NEC Electronics' structured ASIC, *Instant Silicon Solution Platform (ISSP)*, which is being developed to fill the gap between FPGAs and standard cell-based ASICs. The ISSP has a unique regular-fabric architecture designed to achieve both a short time to production and high-performance LSI design. We have developed a special design methodology and tools to fully exploit the capability of this new device. Experimental results for ...

Keywords: ISSP, placement, regular fabric, structured ASIC

16 A parallel bit map processor architecture for DA algorithms

Tom Blank, Mark Stefik, Willem vanCleemput

June 1981 **Proceedings of the 18th conference on Design automation**

Publisher: IEEE Press

Full text available: pdf(748.21 KB)   Additional Information: full citation, abstract, references, citings, index terms

Bit maps have been used in many Design Automation (DA) algorithms such as printed circuit board (PCB) layout and integrated circuit (IC) design rule checking (DRC). The attraction of bit maps is that they provide a direct representation of two-dimensional images. The difficulty with large scale use of bit maps (e.g., for DRC on VLSI) is that the large amounts of data can consume impractical amounts of computation on sequential machines. This paper describes a processing architect ...

17 A layout synthesis system for NMOS gate-cells

J. Luhukay, W. J. Kubitz

January 1982 **Pr ceedings f the 19th c nference n Design aut mati n**

Publisher: IEEE Press

Additional Information:

Full text available: pdf(746.30 KB)   full citation, abstract, references, citings, index terms

A synthesis system for the automatic layout of NMOS gate cells is described. The cells are based on multigrid cell models and are intended for use as part of a chip synthesis system. An outline of the basic concepts of a CAD procedure for the layout synthesis of such cells is given. The main objective is to generate correct and compact cells with controlled growth in area when subjected to modified speed requirements. Both the layout synthesis procedure itself and algorithms are discussed.< ...

18 A new simple and efficient antialiasing with subpixel masks

Andreas Schilling

July 1991 **ACM SIGGRAPH Computer Graphics , Proceedings of the 18th annual conference on Computer graphics and interactive techniques SIGGRAPH '91**, Volume 25 Issue 4

Publisher: ACM Press

Full text available: pdf(647.92 KB)   Additional Information: full citation, abstract, references, citings, index terms

Antialiasing of edges is often performed with the help of subpixel masks that indicate which parts of the pixel are covered by the object that has to be drawn. For this purpose, subpixel masks have to be generated during the scan conversion of an image. This paper introduces a new algorithm for creating subpixel masks that avoids some problems of traditional algorithms, like aliasing of high frequencies or blinking of small moving objects. The new algorithms can be implemented by lookup tables t ...

Keywords: antialiasing, exact area subpixel algorithm

19 Logic fault simulation on a vector hypercube multiprocessor

F. Ozguner, C. Aykanat, O. Khalid

January 1989 **Proceedings of the third conference on Hypercube concurrent computers and applications - Volume 2**

Publisher: ACM Press

Full text available: pdf(847.78 KB)   Additional Information: full citation, abstract, references, citings, index terms

Fault simulation is the process of simulating the response of a logic circuit to input patterns in the presence of all possible single faults and is an essential part of test generation for VLSI circuits. Parallelization of the deductive and parallel simulation methods, on a hypercube multiprocessor and vectorization of the parallel simulation method are described. Experimental results are presented.

20 Temperature and power aware architectures: Integrated architectural/physical planning approach for minimization of current surge in high performance clock-gated microprocessors

Yiran Chen, Kaushik Roy, Cheng-Kok Koh

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(357.09 KB)   Additional Information: full citation, abstract, references, index terms

We propose an integrated architectural/physical planning approach to reduce the power supply noise due to current surge in high performance, general-purpose, clock-gated microprocessors. The proposed approach combines dynamic selection of functional units on-the-fly, dynamic issue width scaling and physical planning with soft module, to balance the current demand across layout. Experimental results show that the proposed approach could reduce the peak noise by 6.54% and consequently, the decoupl ...

Keyw rds: inductive noise, power supply noise

Useful downloads: Adobe Acrobat   QuickTime   Windows Media Player   Real Player

Safari TECH BOOKS ONLINE'

From:ProQuest

US Patent and Trademark Office

Home   Desktop   Library   Safari Labs NEW!   Logout

▼ Search

| lun masking | Go |

☐ Code Fragments only

Advanced Search

▼ Browse By Category

Matching Categories

Networking (37)
   Storage Area
   Network (23)
   IBM TotalStorage (6)
   Tivoli (4)
   More...

Operating Systems (16)
   Linux (6)
   Solaris (2)
   Windows (2)
   More...

Enterprise Computing (7)
   eServer (2)
   Information Storage and
   Retrieval (2)
   IBM LTO Ultrium (1)
   More...

View All Categories...

View All Titles

Applied Sciences
Artificial Intelligence
Business
Certification
Computer Science
Databases
Desktop Applications
Desktop Publishing
E-Business
E-Commerce
Enterprise Computing
Graphics
Hardware
Human-Computer
   Interaction
Internet/Online
IT Management
Markup Languages
Multimedia

Search Results

Found 210 section(s) in 73 book(s) matching your search for "lun masking".

Hide bookcovers

Results: 1 to 5 of

Title	Rank	Relevant Sections	Publisher	Pul
1. Book **Sun Performance and Tuning: Java™ and the Internet, Second Edition** By Adrian Cockcroft, Richard Pettit Slots: 2.0 Table of Contents	★ ★ ★	1. System Configuration Information	Prentice Hall	1!
2. Book **Solaris™ Guide for Windows NT Administrators** By Tom Bialaski Slots: 1.0 Table of Contents	★ ★ ★	1. TCP/IP Troubleshooting Tips	Prentice Hall PTR	1!
3. Book **Designing Storage Area Networks: A Practical Reference for Implementing Fibre Channel SANs** Slots: 1.0 Table of Contents	★ ★ ★	1. Arbitrated Loop	Addison Wesley	1!
4. Book **Fibre Array Storage Technology A FAStT Introduction** By Barry Mellish, Jure Arzensek, Christian Demmer, Noam Rosen Slots: 1.0 Table of Contents	★ ★ ★	1. Storage partitioning and heterogeneous hosts 2. Configuring the FAStT 3. Maintenance, diagnostics and troubleshooting More...	IBM	2(
5. Book **Upgrading and Repairing PCs, 13th Edition** By Scott Mueller Slots: 2.0 Table of Contents	★ ★ ★	1. Glossary	Que	2(

Results: 1 to 5 of

Networking
- Operating Systems
- Programming
- Security
- Software Engineering

▼ Find a Specific Book

- Author
- ISBN
- Title
- Publisher

Related Articles

Safari's related articles offer targeted treatments of technology topics that complement our existing library of more thar articles are written by experts in their fields and presented via trusted sources. Currently in Beta release, O'Reilly Netwc DeveloperWorks are featured as our first sources for this editorial content.

		Title	Source
	Article	**Enhanced Text Input in Windows Forms 2.0**	O'Reilly Network

Safari Guides

Safari Guides deliver notes, tips, warnings and tricks in a variety of key topical areas.

		Title
	Guide	**Photoshop: Create and use a layer mask**
	Guide	**Photoshop: Use Quick Mask to make a selection and refining a selection**

About Safari | Terms of Service | Privacy Policy | Contact Us | Help | Submit a Problem

1003 Gravenstein Highway North
Sebastopol, CA 95472
800-775-7330